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VLSI MINI PROJECT TITLES

S.No:	Project title
1.	Asynchronous fifo controller
2.	ALU (32 operations)
3.	32 bit Parallel CRC
4.	Real Time Clock
5.	Low power cache
6.	A simple DMA controller
7.	I2C communications protocol
8.	SPI communications protocol
9.	Frame assembler and transmitter of Ethernet transmitter
10.	Defer and backoff blocks of Ethernet transmitter.
11.	Multiple scheme arbiter.
12.	Key expansion in AES
13.	Byte substitution in AES
14.	Mix column in AES
15.	AES encryption.
16.	AES decryption.
17.	Uart transmitter
18.	Uart Receiver
19.	IEEE 754-2008 floating point multiplier
20.	Design of N*N matrix multiplication
21.	Design of Manchester encoder and decoder
22.	Implementation of DCT using Verilog HDL
23.	VLSI Design of DES (Data Encryption Standard) Algorithm
24.	Vending machine
25.	Reconfigurable barrel shifter
26.	Baud rate generator
27.	Use of timers in Traffic light controller
28.	8 bit microprocessor
29.	RSA encryption algorithm
30.	MD5 based data integrity system.
31.	Booths multiplier
32.	Efficient on-chip Cross talk avoidance codec design
33.	Energy efficient spatial coding technique for low power applications
34.	Montgomery multipliers.
35.	Command generator for DDR controller
36.	Scheduler for DDR controller.

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37.	Low power LFSR based pattern generator for BIST
38.	MISR based TRA for BIST
39.	Multiple scheme arbiter.
40.	FPGA implementation of low power parallel multiplier
41.	Design of N*N matrix multiplication
42.	Cost efficient SHA hardware accelerators
43.	Binary to seven segment decoder for multiplexed display
44.	DDR memory model implementation
45.	March C+ algorithm (with and without BDS) for MBIST
46.	Design of Content addressable memory.
47.	Fully configurable timer/counter for use in microcontroller.
48.	Vending machine
49.	Binary to bcd and bcd to binary converter
50.	Floating point ALU

	VHDL simulation projects
V1	VHDL implementation of FIR filter structures
V2	Design and Implementation of Asynchronous FIFO for Embedded application
V3	VHDL Implementation of I2C bus Controller
V4	VHDL Implementation of Golay Encoder & Decoder -
V5	CORDIC algorithm for trigonometric function computation in VHDL.
V6	VHDL implementation of efficient source coding technique
V7	Simulation of digital down converter (DDC) in VHDL
V8	Network intrusion detection
V9	VHDL simulation of multi path fading model for broadband wireless networks
V10	VHDL simulation and synthesis of Xilinx FFT IP core for streaming type of signal processing
	VHDL simulation and FPGA kit based projects
F100	FPGA Implementation of UART Controller
F101	FPGA implementation of VGA interface controller
F102	FPGA implementation of DPWM generation circuit
F103	Implementation of stepper motor controller with FPGA.
F104	Implementation of PS/2 Key board interface with FPGA.
F105	Implementation of low cost logic signal analyzer (LSA) on Spartan-3 FPGA.
F106	Study and FPGA implementation of fixed point adders and multipliers structures
F107	FPGA implementation of digital BFSK transmitter and receiver
F108	FPGA Implementation of 32-Bit Arithmetic Logic Unit(ALU) for ARM7 soft

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	processor
F109	FPGA implementation of Distributed Arithmetic based MAC unit
F110	FPGA Implementation of Cyclic Redundancy Check (CRC) generator -
F111	Look up table based digital frequency synthesis for FPGA based applications –
F112	Study and FPGA implementation various PN sequence generators for CDMA communication applications.
F113	FPGA implementation of encryption algorithm for internet applications.
F114	Porting Pico blaze 8 bit soft microcontroller on Spartan 3E FPGA for CSOC applications
F115	Porting Micro blaze 32 bit soft processor on Spartan 3E FPGA using hardware software codesign approach
F116	Implementing fast dual port RAM using block RAMs on Spartan FPGAs
F117	Realizing efficient multi clock domain circuits with digital clock managers (DCMs) of Spartan 3E FPGAs
F118	FPGA realization of Manchester encoder and decoder
F119	Implementing FIR digital filter for FPGA based DSP applications
F120	Implementing Cascade Integer Comb applications for software defined radio applications
F121	Realizing run time configurable FFT core using Xilinx modules on Spartan FPGA
F122	Magnitude computation of complex numbers using area efficient CORDIC algorithm
F123	FPGA implementation of Programmable and reconfigurable timer module for SOC applications
F124	Microwave oven controller built with low cost FPGAs
F125	Simulation, synthesis and FPGA verification of ALU for RISC processor for embedded soft-core applications
F126	Implementation of S-box (Kernel of AES algorithm) for real time on chip cryptography
F127	Implementation of SHA function for FPGA based cryptographic applications
F128	FPGA implementation of Programmable interrupt controller using VHDL
F129	Implementation of hardware Watchdog timer in Xilinx Spartan FPGA
F130	Implementation of real time on chip trace data compression and decompression algorithm

SVS 1	Design of a candy vending machine controller using Verilog HDL
SVS 2	Design of a Escalator and Elevator using Verilog HDL
SVS3	Design of a Asynchronous FIFIO with gray counter using Verilog HDL
SVS4	Design of fire and smoke detector using Verilog HDL with Auto activation of sprinkler

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SVS5	Design and implantation of sequence Detector
SVS6	Design of 16 bit Arithmetic logic unit using Verilog HDL
SVS8	Design of Different real time adders using Verilog HDL
SVS9	Design of RAM with error detection using Verilog HDL
SVS10	Design of Automatic room controller using Verilog HDL
SVS11	Design of siso,sipo,piso,pipo using Verilog HDL
SVS 12	Design of Digital code convertors using Verilog HDL
SVS 13	Design of Digital clock using Verilog HDL
SVS 14	Design of Electronic voting machine using Verilog HDL
SVS 16	Design and implementation of spi using VHDL
SVS 17	Design of Traffic light controller using VHDL
SVS 18	Design of FIR filter using VHDL
SVS 20	Design and implementation of ROM and RAM using VHDL
SVS 21	Design of Round Robin arbiter using VHDL
SVS 22	Design of Barrel shifter using VHDL
SVS 23	Design of Delta to Sigma Convertor using VHDL
SVS 24	Design of Digital Comparator using basic gates using VHDL
SVS 25	Design and implementation of Content Addressable Memory using VHDL
	FPGA implementation of High performance Multiplier using Squarer
	Low power and Area Efficient carry select Adder